

**REMARKS**

Claims 1-3 and 6-8 are pending in this application, claims 6-8 having been withdrawn from consideration. By this Amendment, claims 4, 5 and 9 are canceled without prejudice to or disclaimer of the subject matter contained therein. Claim 1 is amended. Support for the amendment of claim 1 can be found in the specification as filed, for example, at page 8, lines 1-11; page 11, line 27 through page 12, line 7; page 23, line 20 through page 24, line 4; and page 33, lines 2-7. Thus, no new matter is added by this Amendment.

**I. Claim Rejections Under 35 U.S.C. §103(a)****A. Claims 1 and 2**

The Office Action rejects claims 1 and 2 under 35 U.S.C. §103(a) over the combination of Japanese Patent JP-10275905 to Yamamoto and U.S. Patent Application Publication US 2002/0127820 to Sato. Applicants respectfully traverse this rejection.

Claim 1 is directed to a "method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein, after the delamination step, the wafer having an SOI layer is subjected, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer."

Yamamoto, in contrast to claim 1, discloses that a wafer having an SOI layer after the delamination is subjected to a heat treatment by RTA (rapid thermal anneal) in an atmosphere containing hydrogen, which improves the surface roughness of the SOI layer. However, Applicants discovered, for the first time, that RTA only improves the short period

components of surface roughness to a level comparable to that of mirror-polished wafers, and that long period components were still inferior to mirror-polished wafers. Applicants then discovered, for the first time, that in order to improve the long period components of surface roughness, a heat treatment using high heat for a long period of time is required.

Yamamoto performs a heat treatment in hydrogen atmosphere, but does not teach or suggest utilizing both a rapid heating/rapid cooling apparatus and a batch processing type furnace to improve both short periods and long periods of the SOI layer. Thus, Yamamoto alone does not disclose, teach or suggest the invention of claims 1 and 2. Similarly, Sato, alone or combined with Yamamoto, does not disclose, teach or suggest the invention of claims 1 and 2.

Sato discloses the production of SOI wafers and that wafers having an SOI structure are set in a verticle-type hydrogen annealing furnace and subjected to a heat treatment in a hydrogen atmosphere for four hours at 1100°C. See Sato, paragraph [0273]. Thus, although the surface roughness of long periods may be improved by Sato's heat treatment, the surface roughness of short periods is not sufficiently improved.

In addition, the Sato method does not produce an SOI wafer by the hydrogen ion delamination method, as described in claim 1. While the Office Action asserts that Sato discloses implanting hydrogen ions into a semiconductor surface, Sato itself makes clear that a substrate having a porous silicon layer is prepared by the anodization method using hydrofluoric acid, for example, and a nonporous microcrystalline layer is grown on the porous silicon layer, in which hydrogen ions are not implanted into the substrate. Sato's method is thus unlike a hydrogen ion delamination method, such as that described in claim 1. See Sato, paragraphs [0135]-[0138] and [0157]-[0158], Fig. 10A-10E and claims 1 and 2.

Therefore, Sato alone does not disclose, teach or suggest the invention of claims 1 and 2. The combination of Yamamoto and Sato also does not disclose, teach or suggest the invention of claims 1 and 2.

Finding efficiencies that are peculiar to each heat treatment, and discussing that these efficiencies can be retained when the different heat treatments are combined, can be a motivation to combine a heat treatment by an RTA apparatus and that by a batch processing type furnace into a single process. However, such disclosures appear only in the present application. There is no motivation to utilize both a rapid heating/rapid cooling apparatus and a batch type furnace in a single process in either of the cited references. Accordingly, there is no possibility that one of ordinary skill in the art would have been motivated to perform a two-stage heat treatment by utilizing two different types of heat treatment apparatus, as in the claimed invention.

The Office Action asserts that the combination of Yamamoto and Sato teaches annealing by either a furnace or RTA and that, for this reason, it would have been within the scope of one of ordinary skill in the art to use either RTA or furnace heating for the first heating step and the other for the second heating step, having a cooling step in between. Applicants respectfully disagree.

Applicants respectfully submit that the Office Action is selectively combining only the heat treatment processes of Yamamoto and Sato, without any motivation to do so. One of ordinary skill in the art would find that the surface roughness of the SOI layer could be improved by either hydrogen annealing using an RTA or hydrogen annealing using a batch-type furnace. However, without the knowledge or further investigation to discover that the surface roughness of short periods is improved by a rapid heating/rapid cooling apparatus and the surface roughness of long periods of the SOI layer is improved by a batch processing type furnace, even one of ordinary skill in the art would not have been motivated to selectively

combine only the heat treatments of Yamamoto and Sato. That is, because surface roughness generally can be improved by either RTA or batch type furnaces, one of ordinary skill in the art would not perform heat treatments using both RTA and batch type furnaces in which two apparatuses of different types are required and two heat treatment types are required, thereby increasing costs and time for processing. Thus, without a compelling reason, such as the knowledge provided by the present inventors that surface roughness of short periods is improved by rapid heating/rapid cooling apparatus and the surface roughness of long periods is improved by batch type furnaces, such a process would not have been performed.

Neither of the references disclose, teach or suggest that an SOI wafer having an SOI layer is subjected to a two-stage heat treatment by the rapid heating/rapid cooling apparatus after the delamination step, in the atmosphere containing hydrogen or argon.

One of ordinary skill in the art would understand only from the present disclosure that each heat treatment temperature and time (proportion) of RTA and a batch processing type furnace could be optimized for the specific process. That is, without setting the proportion, claims 1 and 2 are distinguishable from the cited art, and further, the surface roughness can be improved in both long and short periods by two-stage heat treatment using two different apparatuses, rather than one stage heat treatment as separately disclosed in each of the cited references.

Further, the Sato method differs completely from the hydrogen ion delamination method of claim 1 and the hydrogen ion delamination method of Yamamoto. Accordingly, there is no motivation in either Sato or Yamamoto to combine only a heat treatment for a wafer after forming an SOI wafer by the method of Sato with the heat treatment of Yamamoto, or vice versa, to produce an SOI wafer since the methods are completely different.

Neither Yamamoto nor Sato contain motivation to combine RTA and a batch processing type furnace; thus, claim 1 cannot be derived from these references. Even if Yamamoto's heat treatment and Sato's heat treatment are combined, the combination cannot lead to claim 1 of this application because claim 1 requires that an SOI wafer having an SOI layer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace, which is clearly different from utilizing either apparatus separately, as disclosed in the cited references.

For at least these reasons, Yamamoto and Sato, alone or in combination, do not teach or suggest the invention of claims 1 and 2. Accordingly, reconsideration and withdrawal of this rejection are requested.

**B. Claims 3-5**

The Office Action rejects claims 3-5 under 35 U.S.C. §103(a) over the combination of Japanese Patent JP-10275905 to Yamamoto and U.S. Patent Application Publication US 2002/0127820 to Sato as applied to claims 1 and 2, and further in view of U.S. Patent 6,074,479 to Adachi et al. and Wolf et al. (Vol. 1). Claims 4 and 5 have been canceled by this Amendment. Accordingly, this rejection is moot as to claims 4 and 5, and Applicants respectfully traverse this rejection with respect to claim 3.

Claim 3 is drawn to a method for producing an SOI wafer by the hydrogen ion delamination method, an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on the surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step.

The Office Action applies Yamamoto and Sato to claim 3 in the same way the references were applied to claims 1 and 2, discussed in detail above. Yamamoto and Sato,

alone or in combination, do not disclose, teach or suggest the invention of claim 3 for at least the same reasons as discussed with reference to claims 1 and 2. The deficiencies of Yamamoto and Sato are not remedied by Adachi and Wolf.

Adachi discloses that wafers stacked up as shown in Fig. 1b are annealed in a furnace so that grown-in defects, which give rise to surface COP and internal COP, are eliminated. See Adachi, col. 1, lines 25-33. Wolf merely discloses that a CZ wafer can be obtained by processing such as slicing a single crystal ingot.

However, there is a problem that the buried oxide layer is etched through COPs in the SOI layer during the hydrogen annealing treatment to form pits if an SOI wafer is produced by using a usual CZ wafer as the bond wafer. See, for example, Specification, page 4, line 12-page 5, line 7; page 6, line 24 - page 7, line 3. But, Applicants discovered that if a wafer without COPs or whose COPs are reduced is used as a bond wafer, as in claim 3, the COPs in SOI layer can be reduced or substantially eliminated, etching of the buried oxide layer due to COPs is not caused, and a heat treatment at a high temperature for a long period of time in a batch processing type furnace becomes possible. See Specification, page 10, lines 3-12, and page 11, lines 12-18. None of the cited references disclose, teach or suggest that when an SOI wafer is produced by the hydrogen ion delamination method, a wafer having reduced COPs is used as the bond wafer.

Specifically, SOI wafers are produced by using as a bond wafer a CZ wafer produced from a single crystal ingot of which grown-in defects, such as COPs, are reduced for the whole crystal by controlling V/G (V: pulling rate, G: temperature gradient along the direction of solid-liquid interface of crystal) (see, for example, Example 3), or an epitaxial wafer (see, for example, Example 4), respectively, and then are subjected to a heat treatment utilizing a batch processing type furnace. See Specification, page 40, line 27 - page 43; Table 3.

Consequently, the surface roughness for both 1  $\mu\text{m}$  square (short periods) and 10  $\mu\text{m}$  square

(long periods) are improved up to the same level as Examples 1 and 2 corresponding to claims 1 and 2. See Specification, Table 2. By producing an SOI wafer by using the wafer recited in claim 3 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere containing hydrogen or argon, generation of pits due to COPs can be prevented and a surface roughness for both short and long periods can be sufficiently improved.

In contrast, none of the cited references disclose, teach or suggest the existence of a problem that the buried oxide layer is etched through COPs in the SOI layer when the SOI wafer after the delamination is subjected to heat treatment in the atmosphere containing hydrogen or argon. Likewise, none of the cited references teach or suggest a solution to the problem, or motivation to combine these references to solve the unspecified problem. None of the references disclose, teach or suggest that generation of pits can be prevented, and none of the references disclose, teach or suggest that a surface roughness for both short and long periods can be sufficiently improved by employing a bond wafer whose COPs in an SOI layer are reduced, and performing a heat treatment in the atmosphere containing hydrogen or argon. Thus, there is no motivation or suggestion in the cited references to use an Adachi CZ wafer as the bond wafer. Likewise, there is no motivation to use the Sato wafer, because Sato produces wafers by the anodization method, rather than the hydrogen ion delamination method. One of ordinary skill in the art would not have been motivated to combine or modify these references to derive the subject matter of claim 3, and the cited references, alone or in combination, do not disclose, teach or suggest the subject matter of claim 3.

Thus, Yamamoto, Sato, Adachi and Wolf, alone or in combination, would not have rendered claim 3 obvious. Accordingly, reconsideration and withdrawal of this rejection is requested.

## II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-3 and 6-8 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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